REMARKS/ARGUMENTS

The present application includes claims 1-7 and 10-19. In the Office Action, the Examiner issued the following restriction requirements:

Species	Figures
I	1-17
II	18-27
III	28-29
IV	30-31

The Examiner deemed that claims 1-2, 10-12 and 14-19 corresponded to Species I. The Examiner deemed that claims 3-4 corresponded to Species II, claims 5-7 corresponded to Species III, and claim 13 corresponded to Species IV. In this amendment, Applicants have amended claim 3 such that claim 3 now corresponds to Species I. Thus, Applicants elect Species I and corresponding claims 1-3, 10-12 and 14-19. Further, Applicants respectfully submit that generic claims 1 and 15 are patentable.

Claim Rejections

The Examiner examined claims based on Applicant's provisional election of Species I and the Examiner's selection of claims corresponding to each species. The Examiner rejected claims 1, 10-11, 15 and 17-18 under 35 U.S.C. §102(b) as being anticipated by Shindo et al. (U.S. Pat. No. 5,048,179). The Examiner rejected claims 2, 12, 14, 16 and 19 under 35 U.S.C. §103(a) as being upatentable over Shindo et al. (U.S. Pat. No. 5,048,179) in view of Nakamura (U.S. Pat. Appl. No. 2007/0166886). The Examiner did not examine claims 3-7 or 13.

Claim 1, 10-11

Applicants amended the first element of claim 1 to add a space in the expression "firstand" to read "first and" and not in response to the Office Action.

The Examiner rejected generic claim 1, and claims 10-11 depending therefrom, as being anticipated by Shindo. Applicants respectfully submit that claim 1 is not anticipated by Shindo. To formulate the 102(b) rejection, the Examiner characterized Shindo by taking Applicant's claim 1 as amended in a first preliminary amendment and adding reference numbers from Shindo. In doing so, the Examiner

mis-characterized Shindo. The Examiner copied the first portion of Applicant's amended claim 1 to characterize Shindo as follows:

> Regarding claim 1, Shindo disclose (e.g. figs. 23-24, see also col. 6/ll. 3 to col. 7/ll. 10) a method for manufacturing an electronic module, comprising: taking a sheet 42, which has a first and a second surface, and which sheet includes an insulating-material layer (plastic) between the first and the second surface, as well as a conductive layer 58 on at least the first surface making at least one recess 46 in the sheet that extends through the second surface and the insulating-material layer as far as the conductive layer 58 on the first surface, which covers the recess from the direction of the first surface (58 of fig. 24) . . .

Applicants dispute the Examiner's characterization. In figs. 23-24 and col. 6/line 3 to col. 7/line 10 Shindo describes a mounting method as follows:

> In the first place, a hole 44 is formed in a plastic substrate 42 for locating therein an IC chip 50. A polyimide film 48 of approximately 12.5 microns thick is adhered to the surface of the substrate 42 with an FEP adhesive layer 46 of 2 to 2.5 microns thick sandwiched between the substrate 42 and the polyimide film 48. Use may, for example, be made of "Kapton" (trademark of du Pont Co.) as the polyimide film 48. Then, an IC chip 50 is located within the hole 44 of the substrate 42 such that the surface of the IC chip 50 is in contact with the FEP adhesive agent layer 46. Then, a filler material 52, e.g., epoxy resin material, is poured into the gap between the hole 44 and the IC chip 50 located within the hole 44 to fill the gap with the filler material 52. Thereafter, as shown in FIG. 24, contact holes 54 and 56 are formed in the polyimide film 48 and FEP adhesive agent layer 46, respectively. In this case, in the first place, the polyimide film 48 is selectively etched by sodium hydroxide, and, thereafter, the FEP adhesive agent layer 46 is etched by an oxygen asher. The resulting contact hole typically has a step, as shown in FIG. 24. An electrically conductive layer 58 is formed in the contact holes 54 and 56 so as to establish an electrical connection between the contact pad of the IC chip 50 and an external circuit (not shown), and this electrically conductive layer 58 is typically formed by deposition of copper to a relatively large thickness of, for example, 5 microns because disconnection could occur at the step portion of the contact hole if this layer is not formed thick enough.

While Shindo does describe a plastic substrate with holes, that is where the similarities between the claimed invention and the Shindo disclosure end. Appliants' claimed method does not include the steps of (1) filling the hole with filler material, (2) providing and adhesive layer on the surface of the plastic substrate, (3) providing an insulating film layer over the adhesive layer, (4) etching holes in the insulating film layer, (5) etching holes in the adhesive layer, and then (6) forming a conductive layer on the insulating film layer that penetrates the holes in the film and

adhesive layers. Further, the method steps disclosed in Shindo must be performed in order. Shindo's improvement is directed to matching the adhesive and insulating layers such that both can be perforated in a single etching step. The method steps disclosed in Shindo necessarily create a gap between the surface of the plastic substrate and the conductive layer and also a "step" which is filled by the conductive layer. According to claim 1, the conductive layer is on the surface of the sheet; therefore, there is not a gap between the surface of the sheet and the conductive layer, and such a gap is also not an inherent result the claimed invention.

For the foregoing reasons, Applicants submit that claims 1 and 10-11 are in condition for allowance. Such action is respectfully requested.

Claims 2, 12 and 14

Applicants amended claim 2 to improve upon the form of the claim and not in response to the Office Action.

The Examiner rejected dependent claim 2, and claims 12 and 14 depending therefrom, under 35 U.S.C. §103(a) as being upatentable over Shindo et al. (U.S. Pat. No. 5,048,179) in view of Nakamura (U.S. Pat. Appl. No. 2007/0166886). Application No. 2007/0166886 is the publication of the present application. Applicants assume that the Examiner intended to refer to U.S. Pat. Appl. No. 2003/0159852 to Nakamura, which reference was submitted by Applicants in an Information Disclosure Statement filed November 14, 2006 and preliminarily respond to the Office Action on that basis. Applicants respectfully request Examiner to either confirm the validity of the Applicant's assumption or withdraw and reissue the Office Action.

Applicants dispute the Examiner's 103(a) rejection. To formulate the 103(a) rejection of claim 2, the Examiner combined Shindo with Nakamura. The references, singly or jointly, do not disclose placing components in recesses in the insulating-layer facing both the first and second surface of the insulating layer. As stated above, the Examiner mis-characterized Shindo. The Examiner also mis-characterized Nakamura and impermissibly used hindsight to combine prior art references. As examined by the Examiner, claim 2 states:

> A method according to Claim 1, wherein the components are placed facing both the first and second surface in the insulating-material layer and electrical contacts are formed to the components in such a way that at least some of the components are connected to the conductive

layer on the first surface and at least some to the conductive layer on the second surface.

Since claim 1 requires placing the components in recesses made in the insulating–material layer, "in the insulating-material layer" necessarily means that at least a portion of each component must be positioned between the first and second surfaces in addition to at least some components being placed facing the first surface and some facing the second surface.

First, the Examiner admitted that "Shindo do not teach the method above, wherein the components are placed facing both the first and second surface in the insulating-material layer and electrical contacts are formed to the components in such a way that at least some of the components are connected to the conductive layer on the first surface and at least some to the conductive layer on the second surface."

Second, Applicants dispute the Examiner's characterization of Nakamura. The Examiner characterized Nakamura as teaching, in fig. 3 and pg. 3/pps. 0037-0044, "the method above, wherein the components 15 or 16 are placed facing both the first and second surface *in the insulating-material layer 11* (glass) and electrical contacts 13 are formed to the components in such a way that at least some of the components are connected to the conductive layer on the first surface and at least some to the conductive layer on the second surface (pg. 3/pp. 0040)." (emphasis added). Nakamura does not disclose *components placed in the insulating-material layer 11.*

Nakamura discloses a multilayer wiring board 1 having a frame resin layer 11 which is a completely cured resin layer, and "a resin layer having built-in components (referred to as 'resin layer 12', hereinafter)." (Page 3, [0040].) Resin layer 12 is semi-cured such that "electronic components 15 and 16 can be buried therein." (Page 3, [0040].) Electronic components are pressed into the semi-cured resin and the resin is then cured. (Page 3, [0043].) Components 15 and 16 are only buried from one side of resin layer 12 and are only electrically connected to that side of resin layer 12. (See any figure.) Applicants have not found any disclosure, either in the specification or the drawings, where Nakamura discloses components buried in resin layer 12 facing <u>both</u> surfaces of resin layer 12.

The Examiner misconstrued the expression "facing both the first and second surface in the insulating-material layer" as <u>only</u> requiring that the components face the first and second surfaces of the insulating-material layer. To place components

facing both the first and second surface of the insulating material 11 (glass), Nakamura requires providing a first resin layer 12 with components facing in one direction, a second resin layer 12 with components facing opposite the one direction, and a resin layer 11 positioned between the first and second layers 12. Thus, the connections on both sides of resin layer 11 connect to components 15 and 16 which are located outside, not between the surfaces of, resin layer 11. Nakamura does not disclose components placed in insulating material 11 (glass), and it does not disclose components placed in an insulating-material layer facing both the first and second surfaces of the insulating-material layer.

Third, the Examiner *prima facie* conclusion of obviousness is necessarily incorrect because it relies on mis-characterization of the prior art references. The Examiner concludes that "since the combination of Shindo and Nakamura *teach the method above*, it would have been obvious to a have . . . for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components." (emphasis added). As discussed above, the combination of Shindo and Nakamura do not teach the method above.

Finally, even if Shindo and Nakamura had taught the method above, the Examiner's *prima facie* conclusion is based on impermissible hindsight as the Examiner does not articulate a reason with rational underpinning to support the conclusion. "[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex Inc.,* 127 S.Ct. 1727, 1741 (2007); see also MPEP § 2141 (2007). Applicants disclose in page 2 of U.S. Pat. Appl. No. 2007/0166886, which was cited incorrectly by the Examiner, at paragraph [0010] "[t]he invention is intended to create a simple and reliable method with low malfunctioning costs, for embedding components in an installation base." The benefit cited by the examiner was provided by the Applicant and is, consequently, hindsight. The Examiner has provided no reason predating the applicant's invention to support combining the prior art references.

For the foregoing reasons, Applicants submit that claims 2, 12 and 14 are in condition for allowance. Such action is respectfully requested.

Claim 3

Applicants amended claim 3 such that claim 3 now corresponds to Species I. Applicants incorporated the limitations of claim 1 such that claim 3 is now an independent claim. Applicants also added limitations directed to gluing a component to the conductive layer on the second surface with the aid of electrically insulating adhesive and making feed-throughs to the second component. For the foregoing reasons, Applicants submit that claim 3 is in condition for allowance. Such action is respectfully requested.

Claims 4-7 and 13

Claims 4-7 and 13 depend, directly or indirectly, from claim 1. Applicants submit that claim 1, and therefore claims 4-7 and 13, are in condition for allowance. Such action is respectfully requested.

Claims 15, 17-18

The Examiner rejected claim 15, and claims 17-18 depending therefrom, as being anticipated by Shindo. Claim 15 recites:

> 15. An electronic module, comprising:
> a sheet, which has a first and a second surface, and which sheet includes an insulating-material layer between the first and the second surface,
> a conductive pattern layer on at least the first surface of the sheet,
> at least one recess in the sheet that extends through the second surface and the insulating-material layer as far as the conductive pattern layer on the first surface of the sheet,
> a component having a contact surface with contact areas or contact protrusions, the component placed in the recess with the contact surface of the component facing the first surface,
> an electrically insulating adhesive attaching the component to the conductive pattern layer on the first surface of the sheet, and
> feed-throughs connecting at least some of the contact areas or contact protrusions of the component electrically to the conductive pattern layer on the first surface of the sheet.

As discussed with reference to claim 1, the method steps disclosed in Shindo necessarily create a gap between the surface of the plastic substrate and the conductive layer. The method also creates a "step" which is filled by the conductive layer. According to claim 15, the conductive layer is on the surface of the sheet;

therefore, there is not a gap between the surface of the sheet and the conductive layer, and such a gap is also not an inherent result the claimed invention. Consequently, Shindo does not anticipate claim 15 because it does not provide a sheet having a conductive pattern layer on at least the first surface of the sheet.

For the foregoing reasons, Applicants respectfully submit that claim 15, and consequently dependent claims 17-18, are in condition for allowance. Such action is respectfully requested.

Claims 16 and 19

The Examiner rejected claims 16 and 19 under 35 U.S.C. §103(a) as being upatentable over Shindo in view of Nakamura. Applicants incorporated the limitations of claim 15 into claim 16 such that claim 16 is now an independent claim. Applicants also added to claim 16 limitations directed to electrically insulating adhesive and feed-throughs. Claim 19 depends from claim 15. For the same reasons stated above with respect to claims 2 and 15, Applicants respectfully submit that claims 16 and 19 are patentable over Shindo and Nakamura.

Applicants believe that a three month extension of time fee and no other fee is required for the submission of this Amendment. Please charge the three month extension of time fee and, if Applicant's belief is in error, any other fees which may be due to Baker & Daniels' Deposit Account No. 02-0390. Any such fees charged to Deposit Account No. 02-0390 should not include the payment of issue fees for this application.

Respectfully submitted,

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